

# Claims

- [c1] 1. A method of expanding pins of a chip for using first interface of a first chip to transfer pins of a second interface of the first chip to a second chip, comprising:  
encoding a second interface command transmitted by a second interface of a first chip into a first interface command, wherein the first interface command can be transmitted by a first interface of the first chip; and  
receiving the encoded first interface command and decoding the first interface command into the second interface command, wherein the first interface command is received by a second chip so that pins of the second chip can transmit the second interface command.
- [c2] 2. The method of expanding pins of a chip of claim 1, wherein the first chip is a DVD or VCD player chip.
- [c3] 3. The method of expanding pins of a chip of claim 1, wherein the second chip is a memory chip.
- [c4] 4. The method of expanding pins of a chip of claim 1, wherein the first interface is an address/data bus.
- [c5] 5. The method of expanding pins of the chip of claim 1, wherein the second interface is a general-purpose input/

output (GPIO).

- [c6] 6. A chip for expanding pins of a chip, comprising:
  - a core logic;
  - a multiplexer;
  - a controller, coupled to the core logic and the multiplexer, adapted for receiving a command from the core logic to transmit a first interface command;
  - a command encoder, coupled to the core logic and the multiplexer, adapted for receiving a second interface command and encoding the second interface command into the first interface command; and
  - an arbitrator, coupled to the core logic and the multiplexer, adapted for controlling the multiplexer and selectively transmitting the first interface command of the controller or the command encoder.
- [c7] 7. The chip for expanding pins of a chip of claim 6, wherein the core logic is an audio/video player logic.
- [c8] 8. The chip for expanding pins of a chip of claim 6, wherein the controller is a memory controller.
- [c9] 9. The chip for expanding pins of a chip of claim 6, wherein the first interface command is a memory access command.
- [c10] 10. A memory chip, comprising:

a memory circuit;  
an address decoder, coupled to the memory circuit,  
adapted for receiving a memory access command and  
transmitting the memory access command according to  
a access address of the memory access command; and  
a command decoder, coupled to the address decoder,  
adapted for decoding the memory access command  
transmitted by a second interface.

[c11] 11. The memory chip of claim 10, wherein the second  
interface is a general-purpose input/output (GPIO).